CIN' (consistant with description).

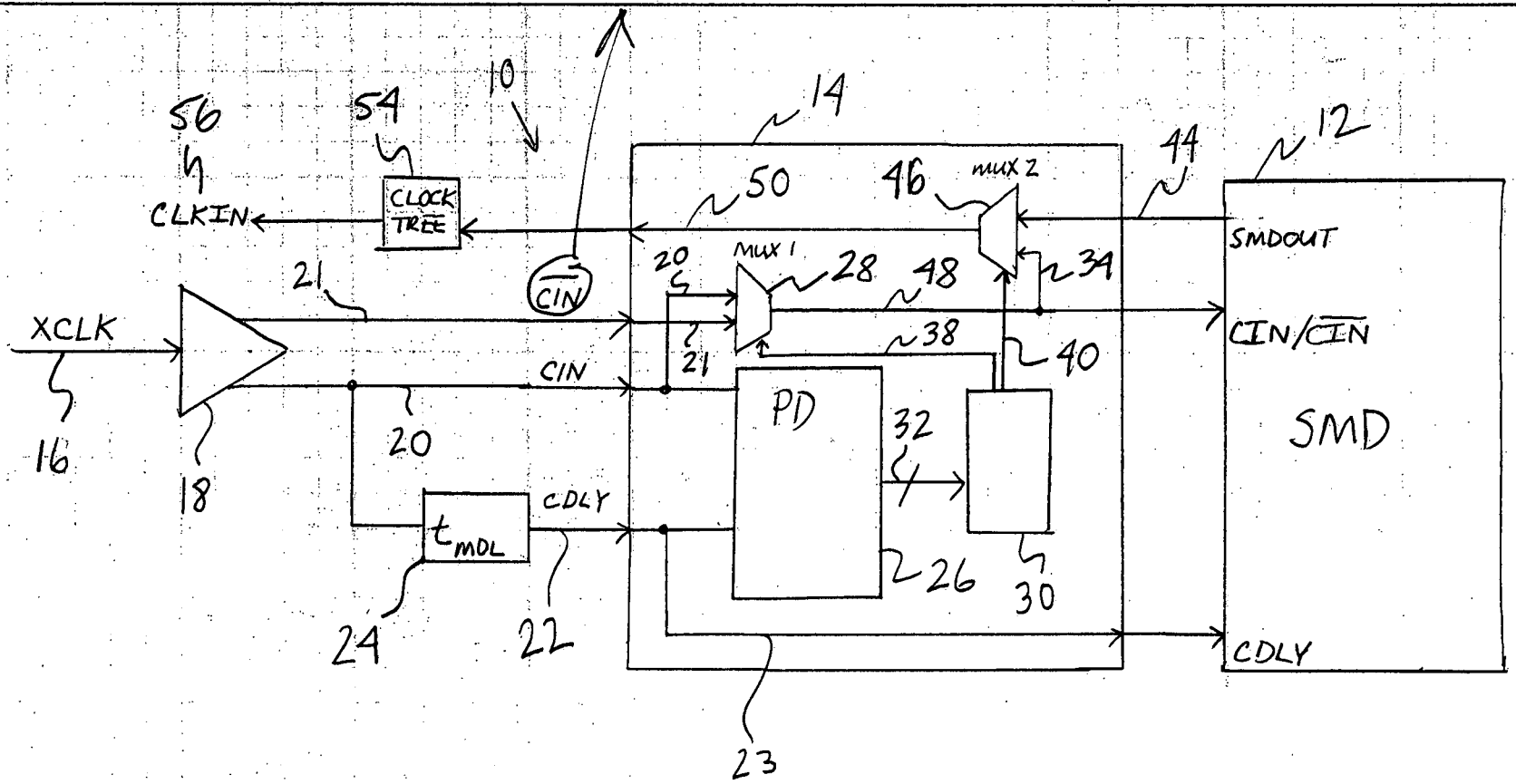

FIG. 1

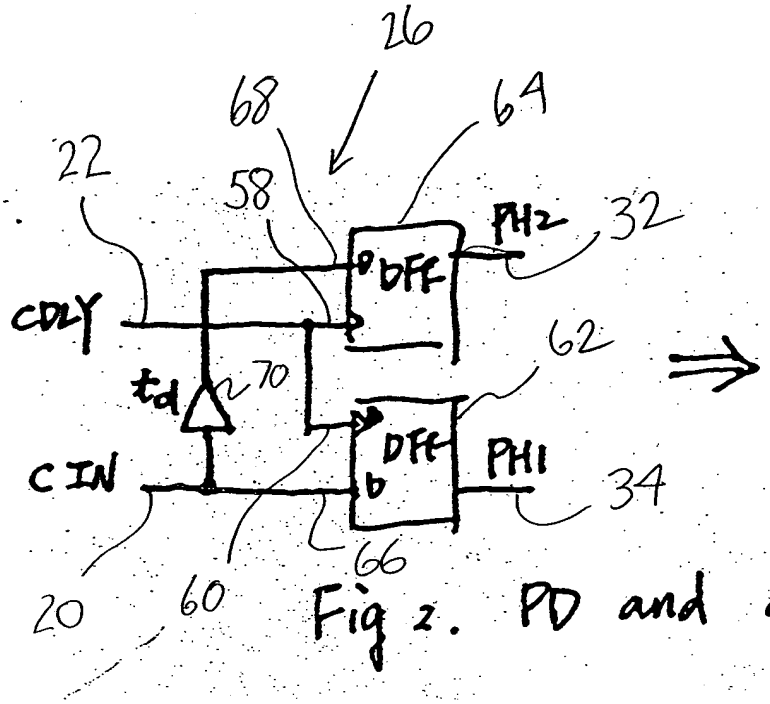

Fig 2. PD and conditions

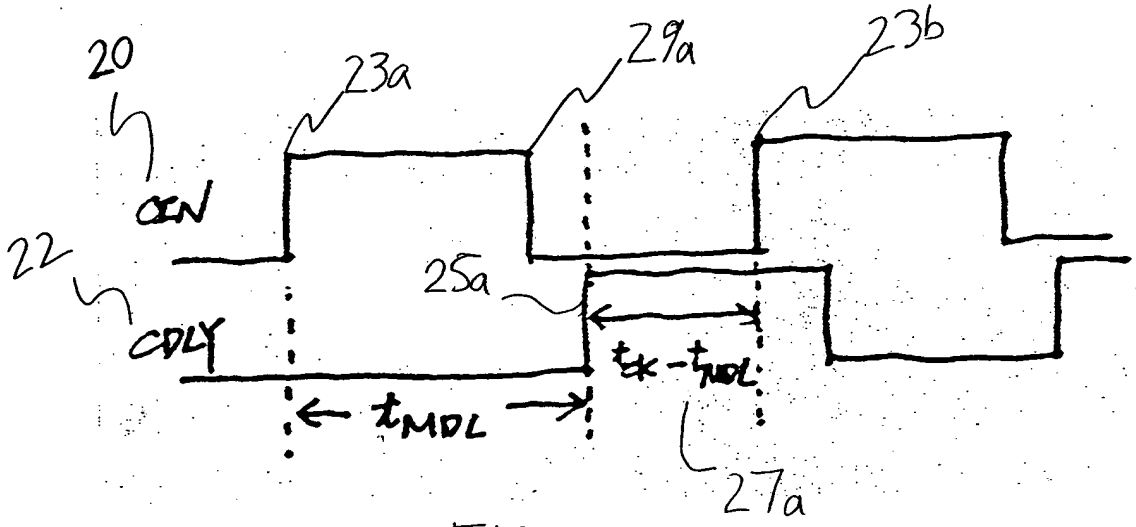

FIG. 3

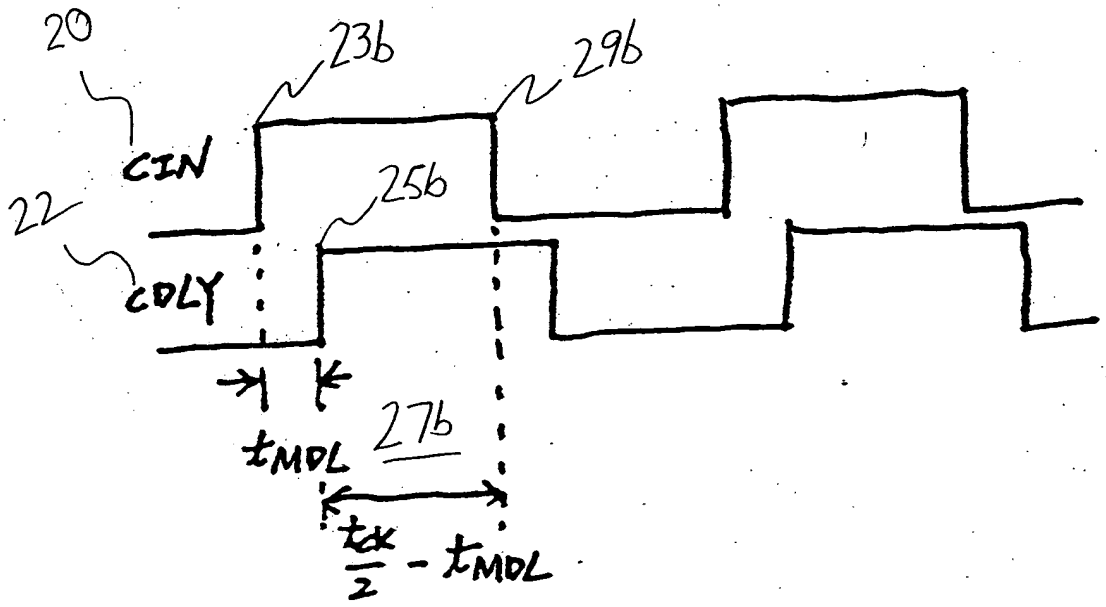

FIG. 4

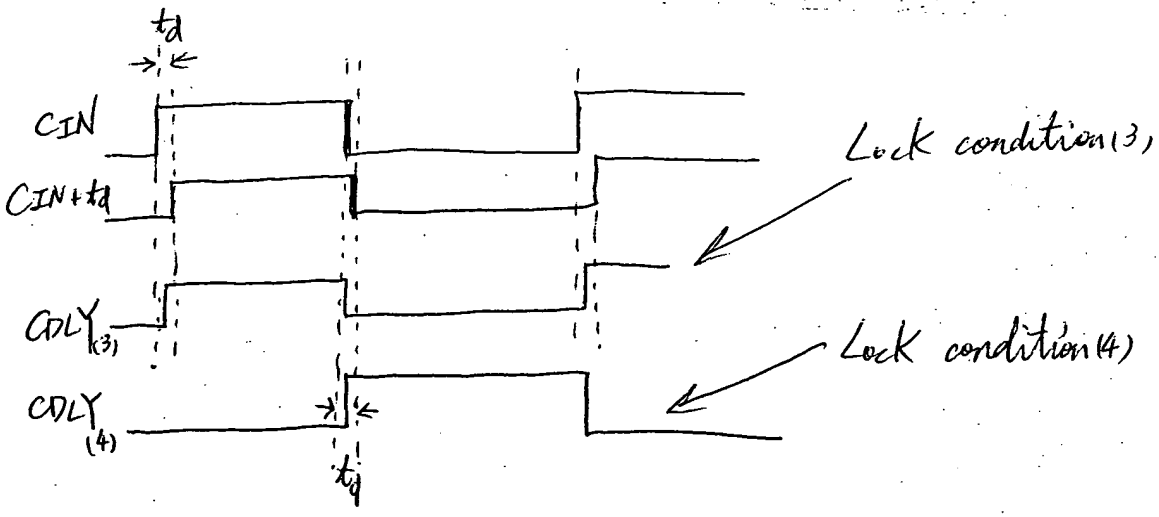
td
CIN
CIN+td
CDLY(3)
CDLY(4)
td
Lock condition(3)
Lock condition(4)

FIG. 4a

	PH1 (32)	PH2 (34)	Conditions	
(1)	0	0	$t_{CK} - t_{MDL}$	($t_{MDL} > \frac{t_{CK}}{2}$)
(2)	1	1	$\frac{t_{CK}}{2} - t_{MDL}$	($t_{MDL} < \frac{t_{CK}}{2}$,
(3)	1	0	$t_{MDL} = t_{CK}$	(locked)
(4)	0	1	$t_{MDL} = t_{CK}/2$	(locked IE

FIG. 5

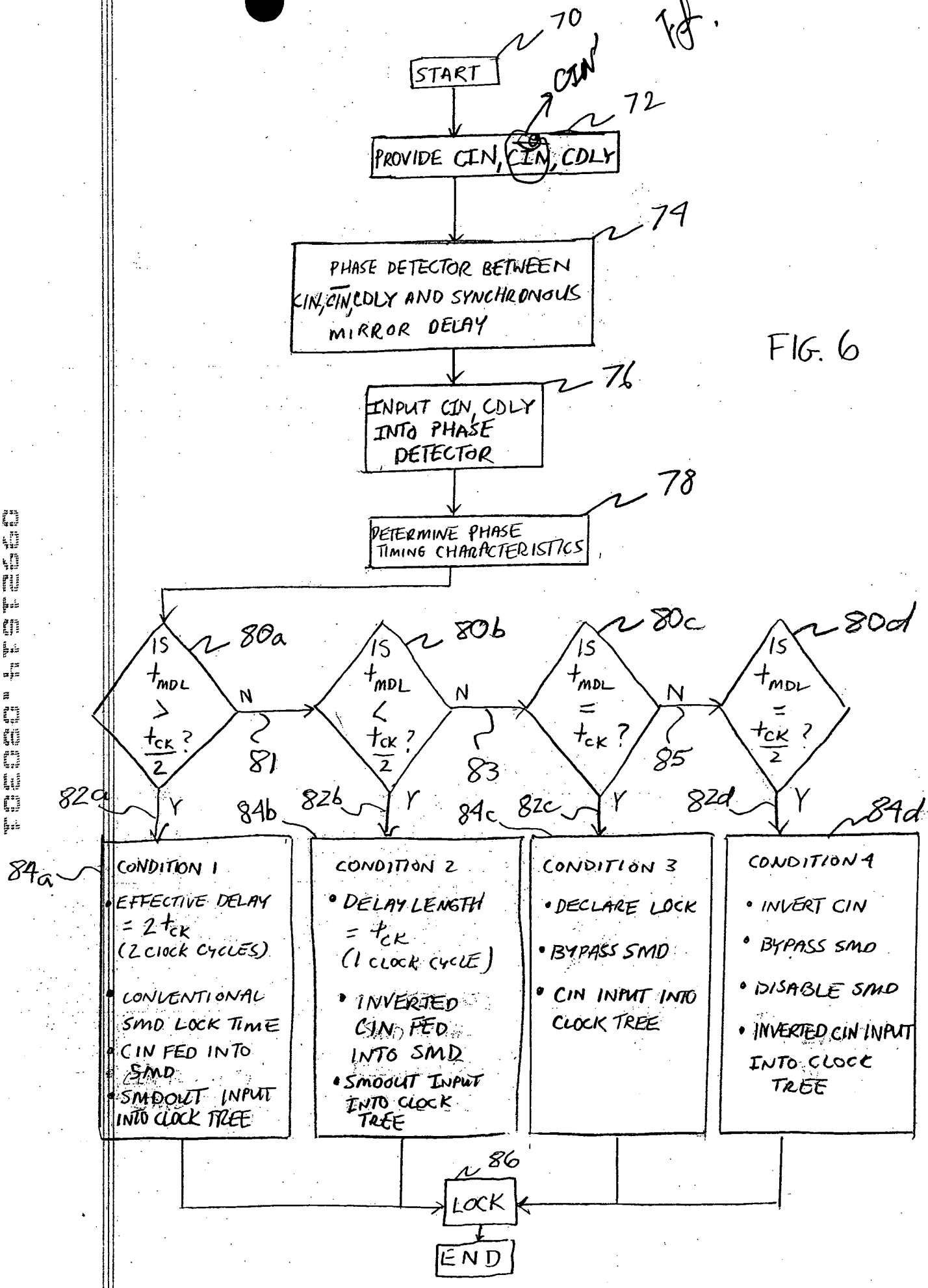
70
START
CIN
72
PROVIDE CIN, $\overline{CIN}$, CDLY
74
PHASE DETECTOR BETWEEN CIN, $\overline{CIN}$, CDLY AND SYNCHRONOUS MIRROR DELAY
76
INPUT CIN, CDLY INTO PHASE DETECTOR
78
DETERMINE PHASE TIMING CHARACTERISTICS
80a
IS $t_{MDL} > \frac{t_{CK}}{2}$?
N
81
80b
IS $t_{MDL} < \frac{t_{CK}}{2}$?
N
83
80c
IS $t_{MDL} = t_{CK}$?
N
85
80d
IS $t_{MDL} = \frac{t_{CK}}{2}$?
82a
Y
82b
Y
82c
Y
82d
Y
84a
CONDITION 1
• EFFECTIVE DELAY = $2t_{CK}$ (2 CLOCK CYCLES)
• CONVENTIONAL SMD LOCK TIME
• CIN FED INTO SMD
• SMDOUT INPUT INTO CLOCK TREE
84b
CONDITION 2
• DELAY LENGTH = t_{CK} (1 CLOCK CYCLE)
• INVERTED CIN FED INTO SMD
• SMDOUT INPUT INTO CLOCK TREE
84c
CONDITION 3
• DECLARE LOCK
• BYPASS SMD
• CIN INPUT INTO CLOCK TREE
84d
CONDITION 4
• INVERT CIN
• BYPASS SMD
• DISABLE SMD
• INVERTED CIN INPUT INTO CLOCK TREE
86
LOCK
END

FIG. 6

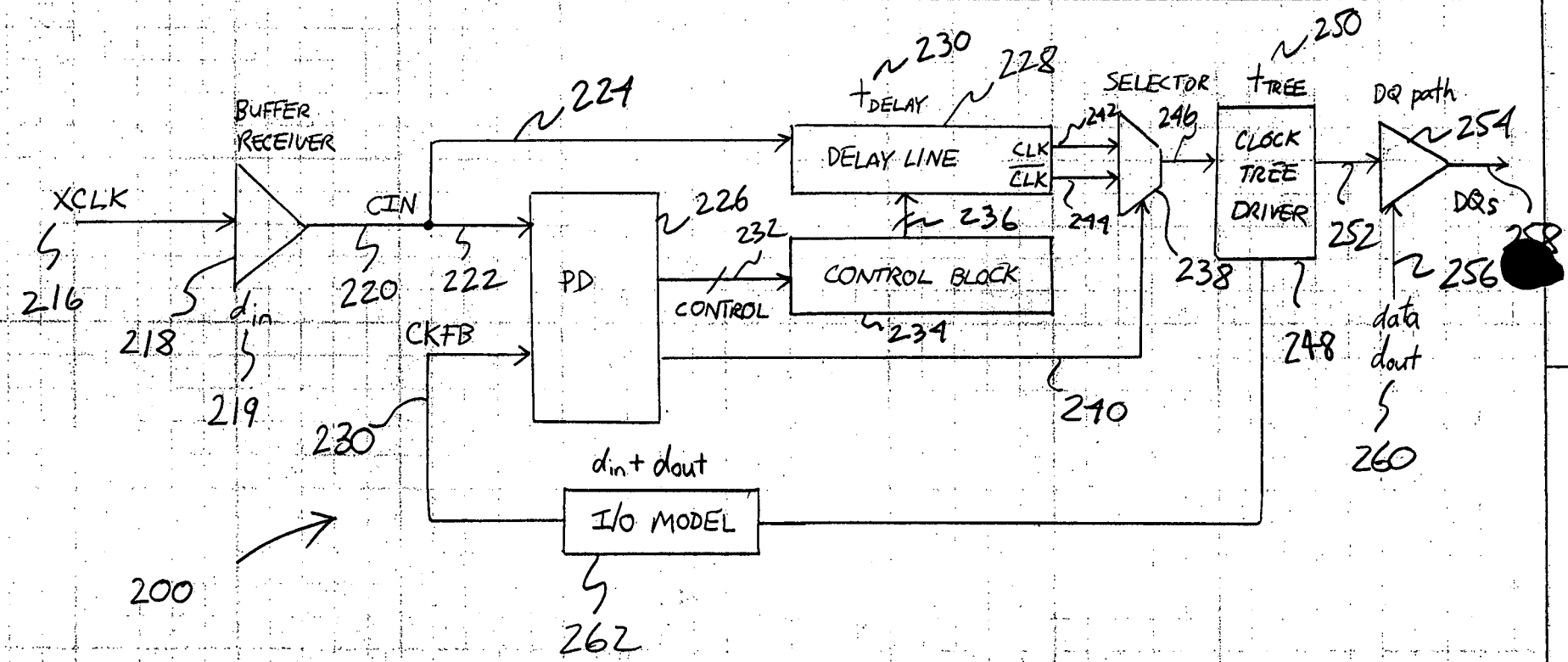

FIG. 7

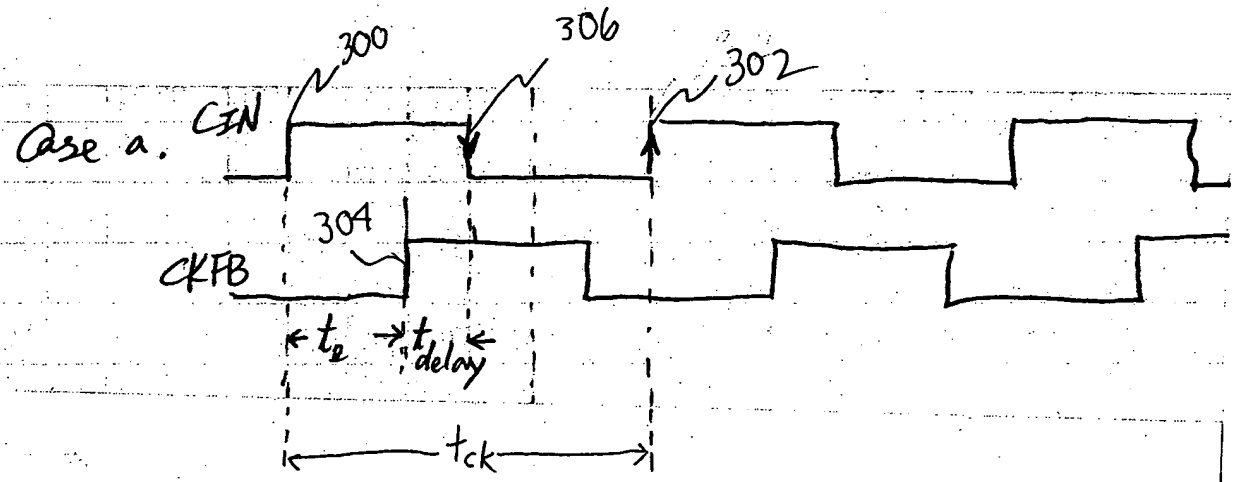

FIG. 8

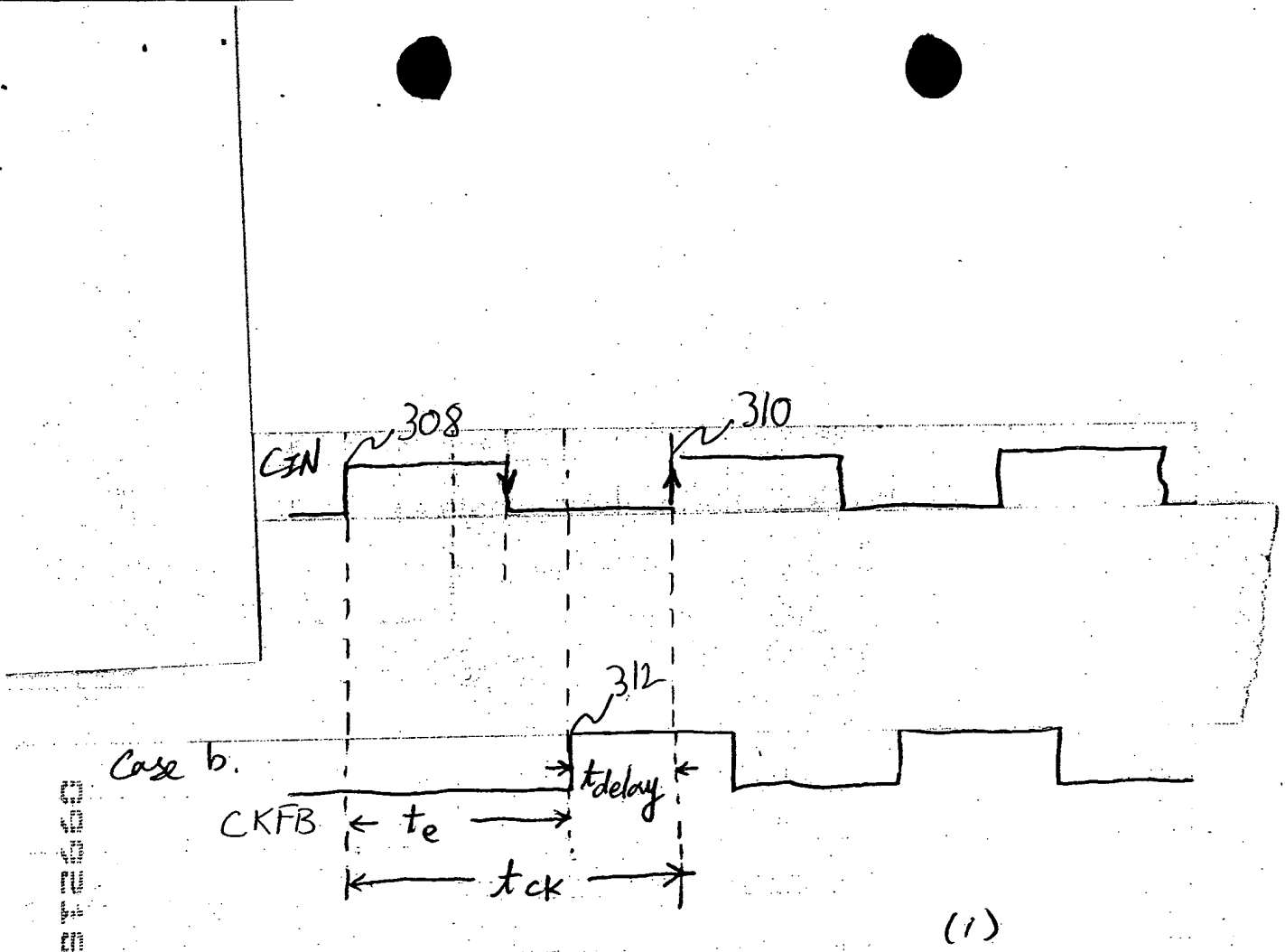

FIG. 9

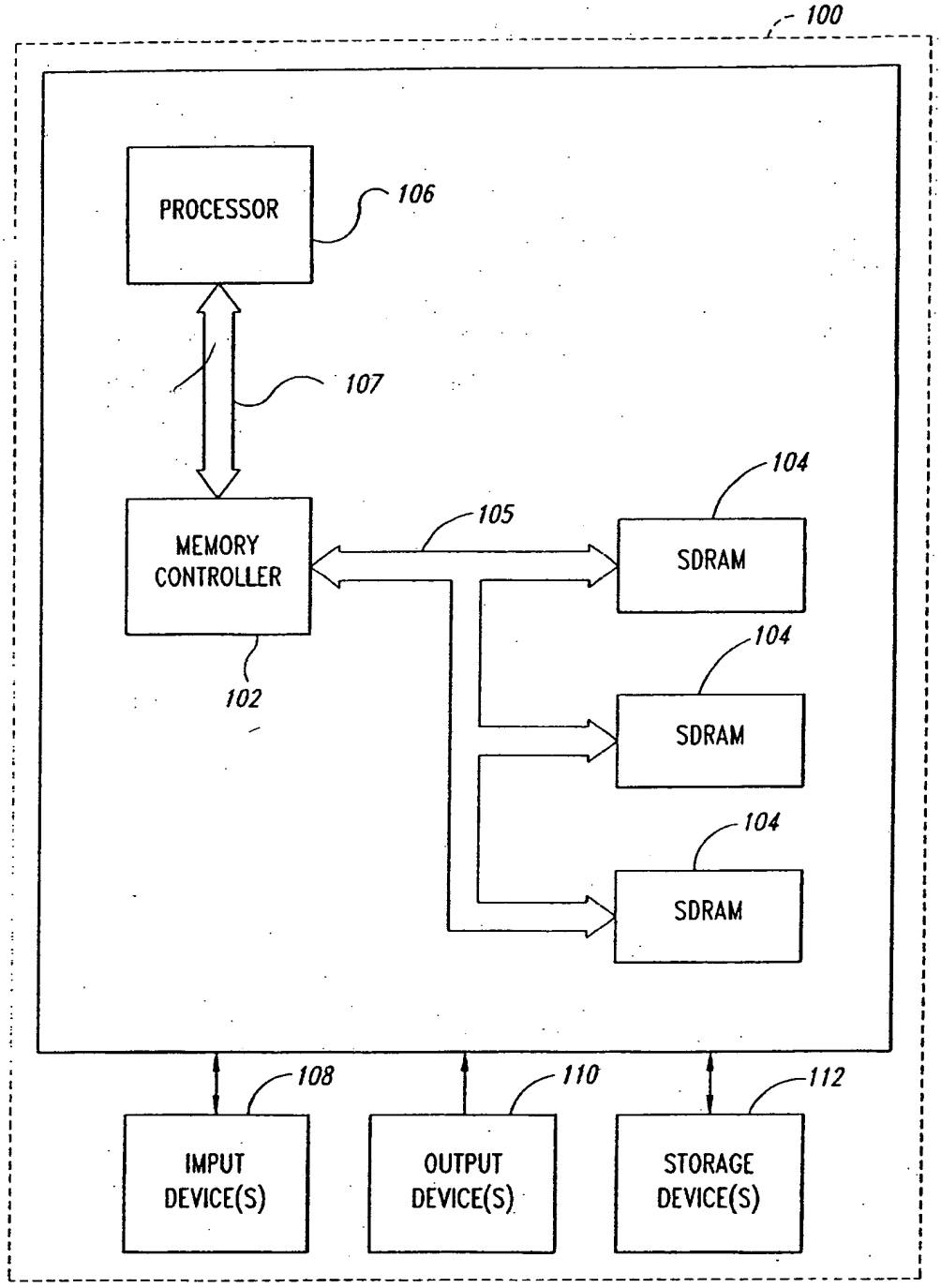
100
PROCESSOR
106
107
MEMORY CONTROLLER
105
102
104
SDRAM
104
SDRAM
104
SDRAM
108
IMPUT DEVICE(S)
110
OUTPUT DEVICE(S)
112
STORAGE DEVICE(S)

Fig. 10